



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Toshifumi MORI et al.**

Group Art Unit: **TBA**

Serial No.: **10/694,359**

Examiner: **Unassigned**

Filed: **October 28, 2003**

Confirmation No.: **TBA**

For: **METHOD FOR FABRICATING SEMICONDUCTOR DEVICE**

Attorney Docket No.: **032068**

Customer Number: **38834**

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 CFR 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

January 5, 2004

Sir:

Applicants direct the attention of the Patent and Trademark Office to the documents listed on the attached Form PTO-1449. A copy of each listed document is attached.

No fee or certification is required in connection with this Information Disclosure Statement, because it is being submitted prior to the issuance of a first official action on the merits or expiration of the three month period following the filing date or the entry of the national stage of the above-captioned application.

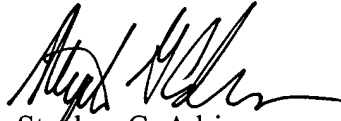
The above information is presented so that the Patent and Trademark Office can, in the first instance, determine any materiality thereof to the claimed invention. Applicants respectfully request that the information be expressly considered during the prosecution of this application and that the documents cited in the attached Form PTO-1449 be made of record therein and appear on the first page of any patent to issue therefrom.

Information Disclosure Statement
Attorney Docket No. 032068
Serial No.10/694,359

The Commissioner is authorized to charge our Deposit Account No. 50-2866 for any fee that is required to effect consideration of this statement.

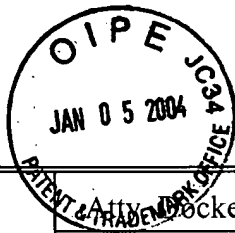
Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

A handwritten signature in black ink, appearing to read 'Stephen G. Adrian', is written over the printed name.

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INFORMATION DISCLOSURE CITATION PTO-1449	Patent No. 032068	Serial No. 10/694,359
	Applicant(s): Toshifumi MORI et al.	
	Filing Date: October 28, 2003	Group Art Unit: TBD

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Country	Translation (Yes or No)

OTHER DOCUMENTS

		Wei W. Lee, et al.; FABRICATION OF 0.06 μm POLY-Si GATE USING DUV LITHOGRAPHY WITH A DESIGNED $\text{Si}_x\text{O}_y\text{N}_z$ FILM AS AN ARC AND HARDMASK ; 1997 Symposium on VLSI Technology Digest of Technical Papers; pp. 131 & 132; 1997.
Examiner		Date Considered